RISC-V Multi-Cycle Core Vector Accelerator

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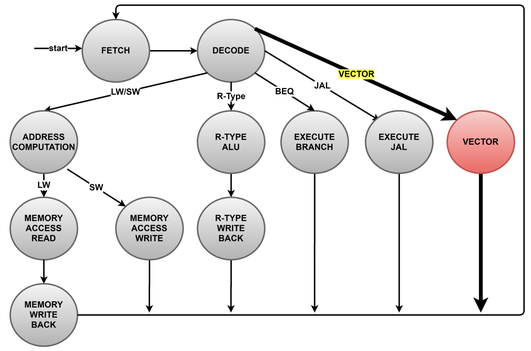
Background

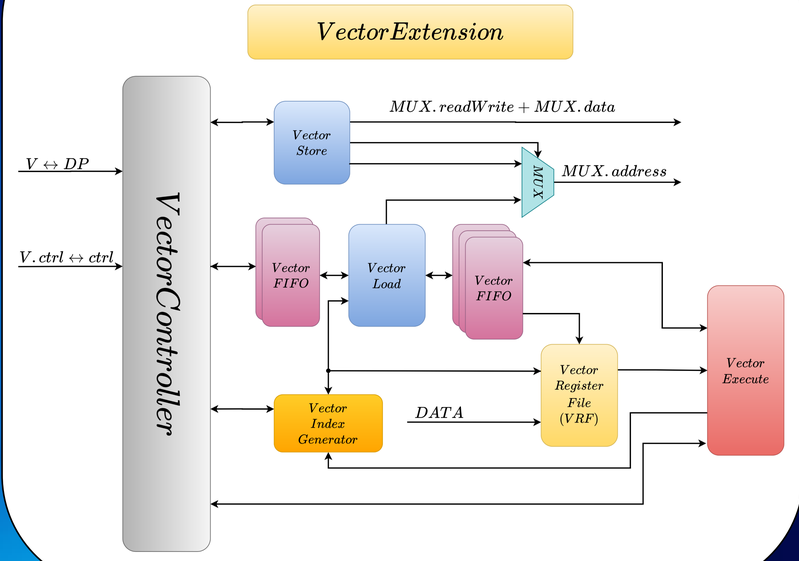
- Vector calculations have become more and more essential, especially in fields of machine learning. Execution of those calculations can be done using Vector-Instructions, which can be found in the vector extension ISA of RISC-V.
- Nowadays, the majority of VPUs are attached to pipeline microarchitecture. That integration is complicated, so in many cases, for simplicity, the pipeline is replaced with a single-cycle microarchitecture. In order to build a machine or accelerator that executes mostly vector instructions, we present a new approach, the attachment of a VPU to a RISC-V Multi-Cycle microarchitecture core.

Project Scope

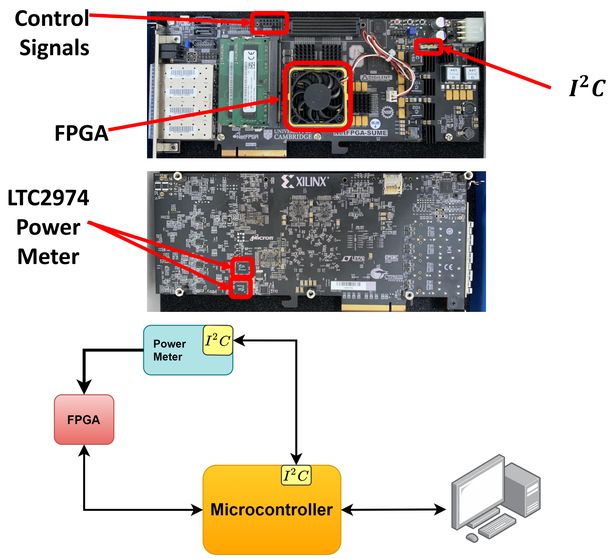
- Explore "Vector Extension" in the environment of a RISC-V Multi-Cycle core.
- RISC-V Vector Processor From A to Z: Design, Implement, Validate, and Evaluate.



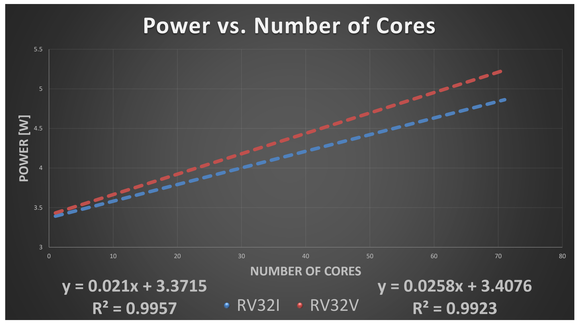
VPU Design



Performance Measurement System



Results



Parameter	Integer Core -RV32I	Vector Processor -RV32V	$\frac{Integer}{Vector}$
Hardware Complexity			0.25
Power	21 [mW]	26 [mW]	0.8
Time Per Program	325 [µs]	31 [µs]	10.5
Energy Per Program	6,825 [nJ]	806 [nJ]	8.5
Figure of Merit[1]	88.8		

Conclusions

This project confirms that the RISC-V Multi-Cycle microarchitecture is a proper host for vector processing. We found the combination of the two fruitful and turned the non-efficient Multi-Cycle microarchitecture into an efficient vector processing machine, our RISC-V Vector Processor. For the cost of hardware complexity, we gained substantial improvement in both execution time and energy consumption. We also developed a performance measurement system that enabled us to measure the execution time and power consumption of our design. Our system can be adopted by every project that will make use of the NetFPGA-SUME development board.