ANDREW AND ERNA VITERBI FACULTY OF ELECTRICAL ENGINEERING

THE PROF. ISRAEL CEDERBAUM HIGH SPEED DIGITAL SYSTEMS LABORATORY HS DSL המעבדה למערכות ספרתיות מהירות ע"ש פרופ' ישראל צדרבאום

Technion Israel Institute of Technology

Vector Accelerator for RISC-V

Oded Eini and Lionn Bruckstein

Instructor: Professor Ran Ginosar

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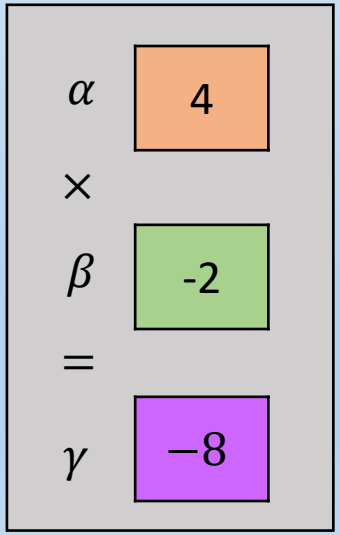
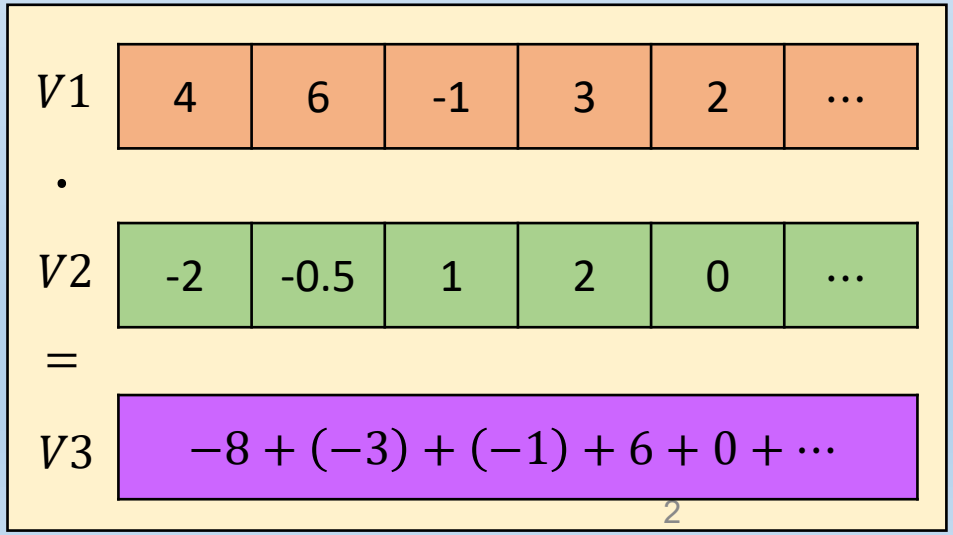
Background

- Integer Instruction `mul x2 x5 x8` # $\gamma = \alpha \times \beta$
- Vector Instruction `v.madd x6 x7 x10` # $V3 = V1 \cdot V2$
- Vector Processor



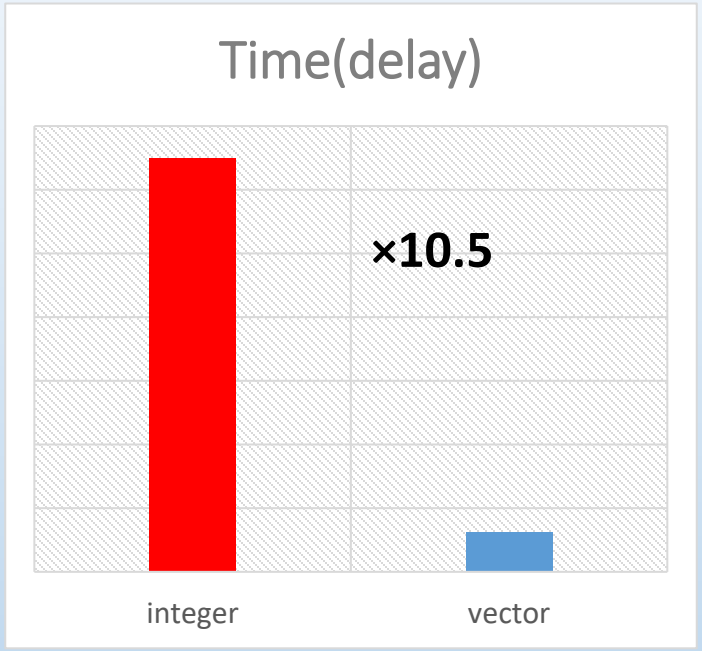


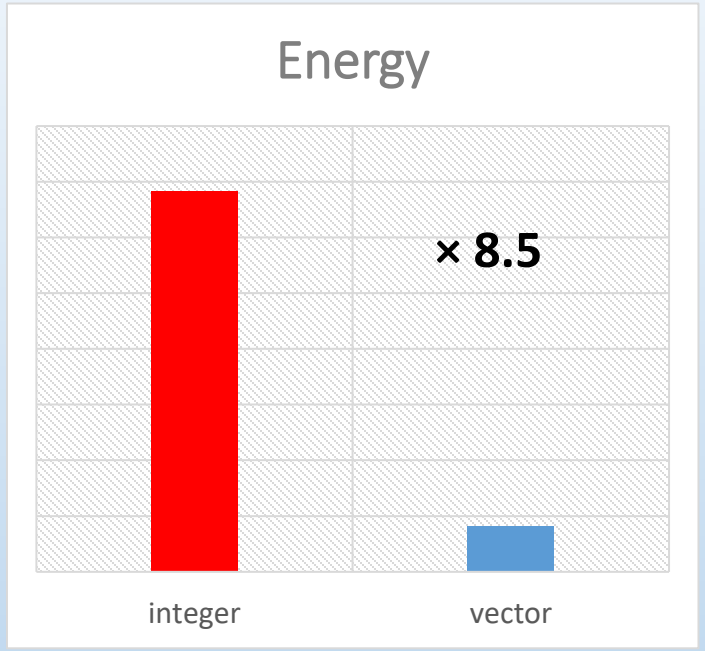
Motivation

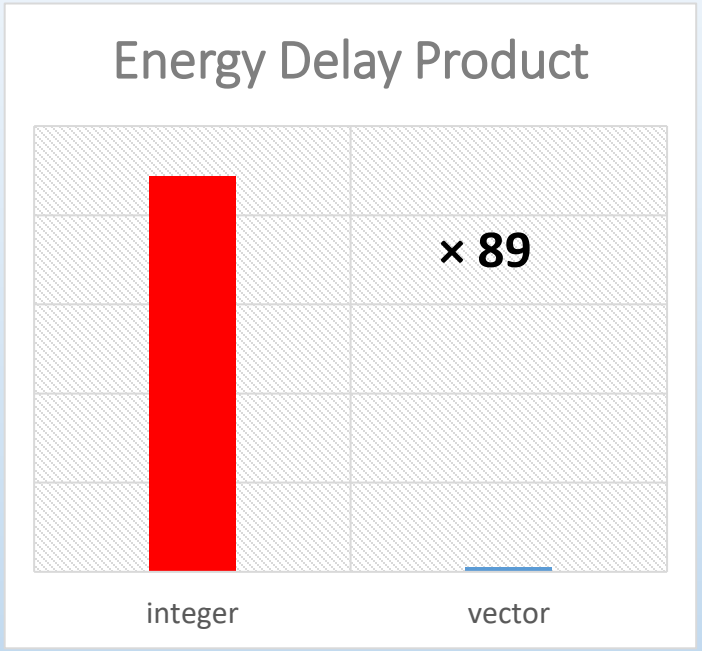
- Growing need for vector processors: machine-learning, DSP, etc.
- Nowadays implemented into Pipeline = Complicated
- Multi-Cycle Microarchitecture

Has Never Been Explored Before

Let Us Begin From the End



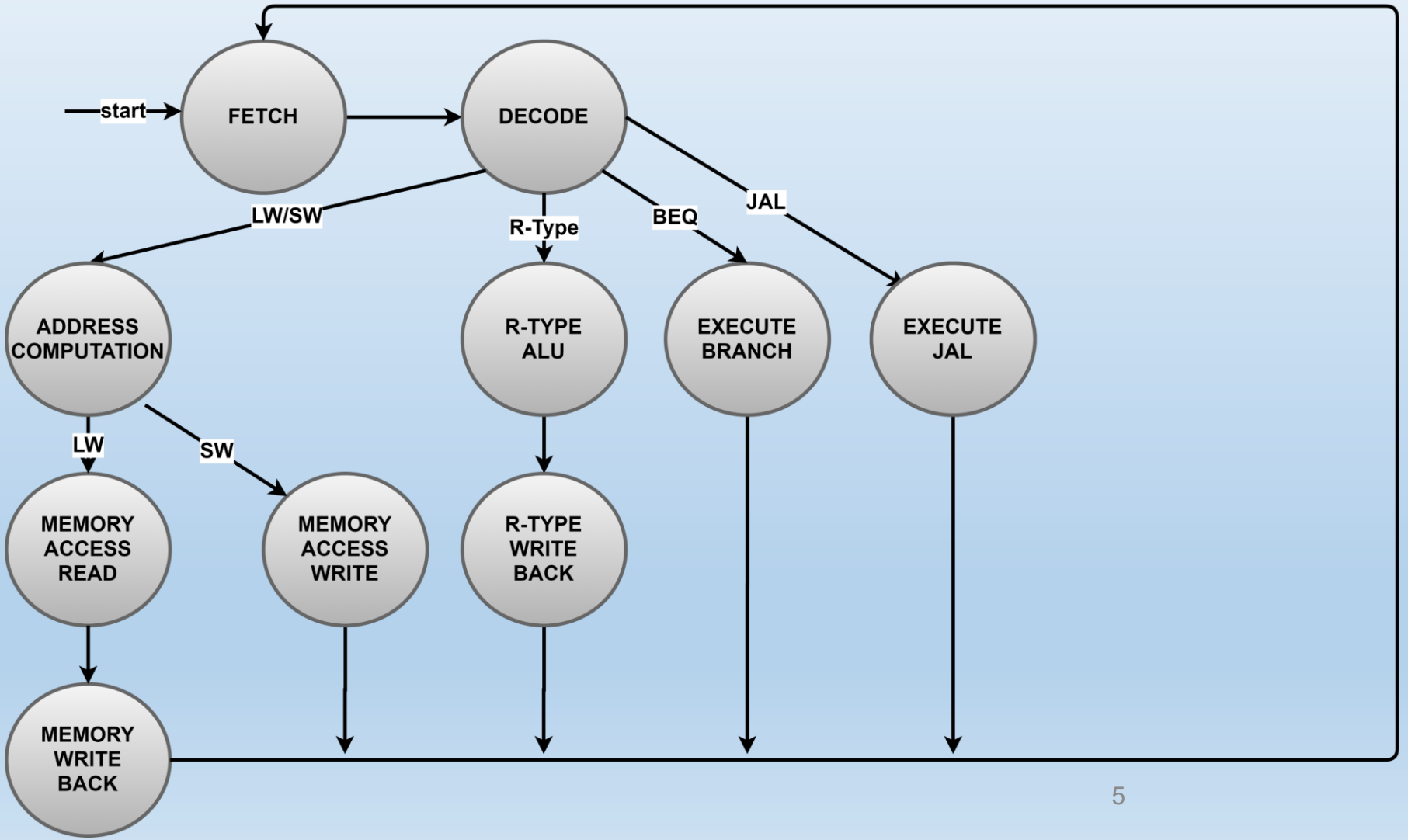




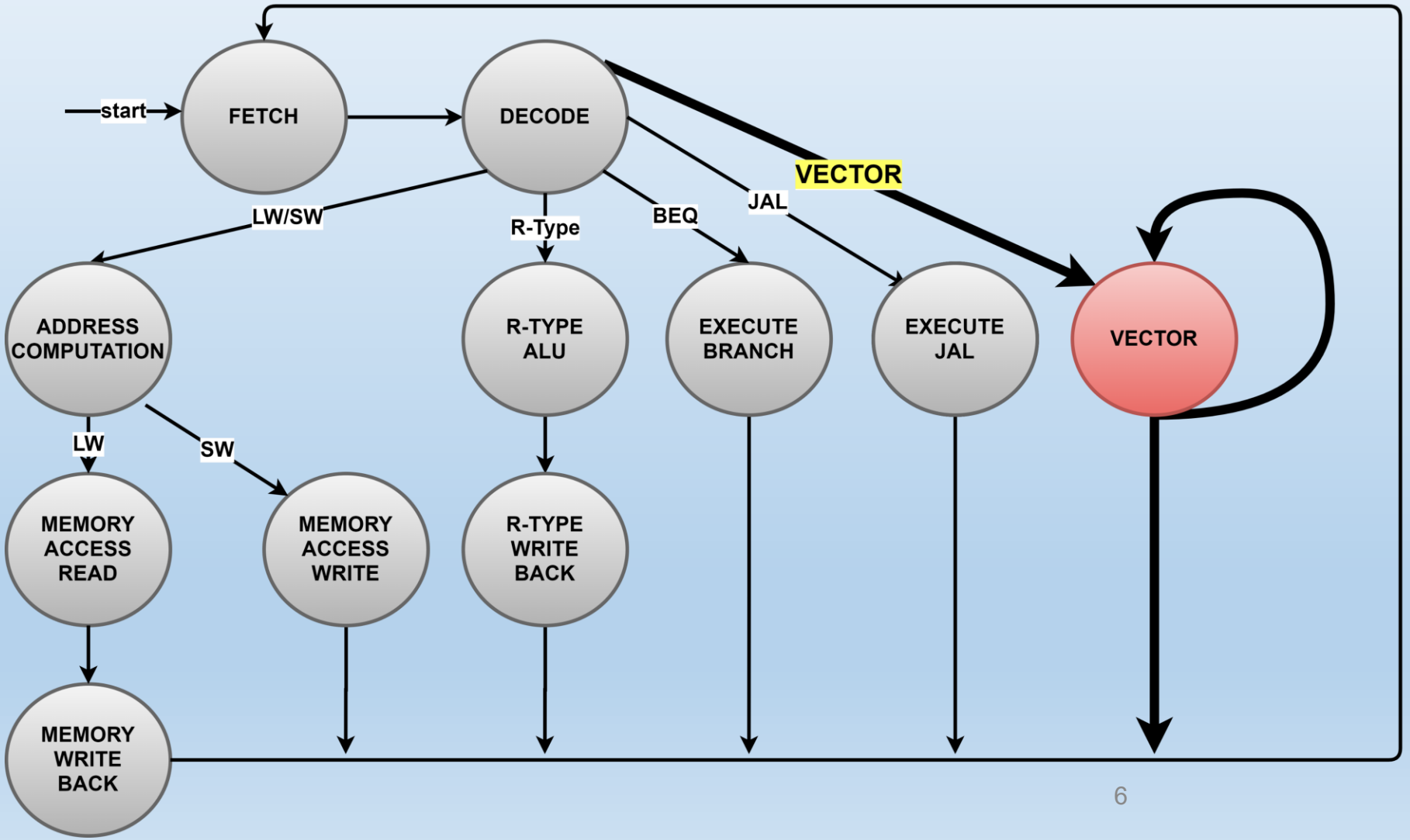
1. Vector processor is faster and more energy efficient

2. Easier to implement with Multi-Cycle than with Pipeline

RISC-V Multi Cycle FSM

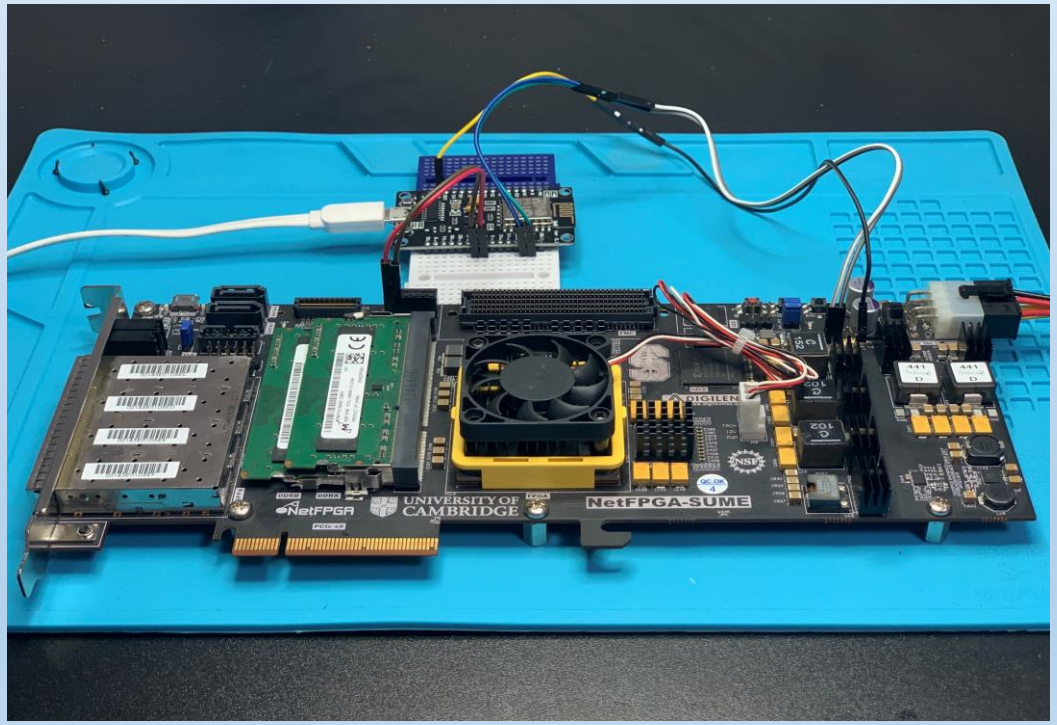


RISC-V Multi Cycle FSM



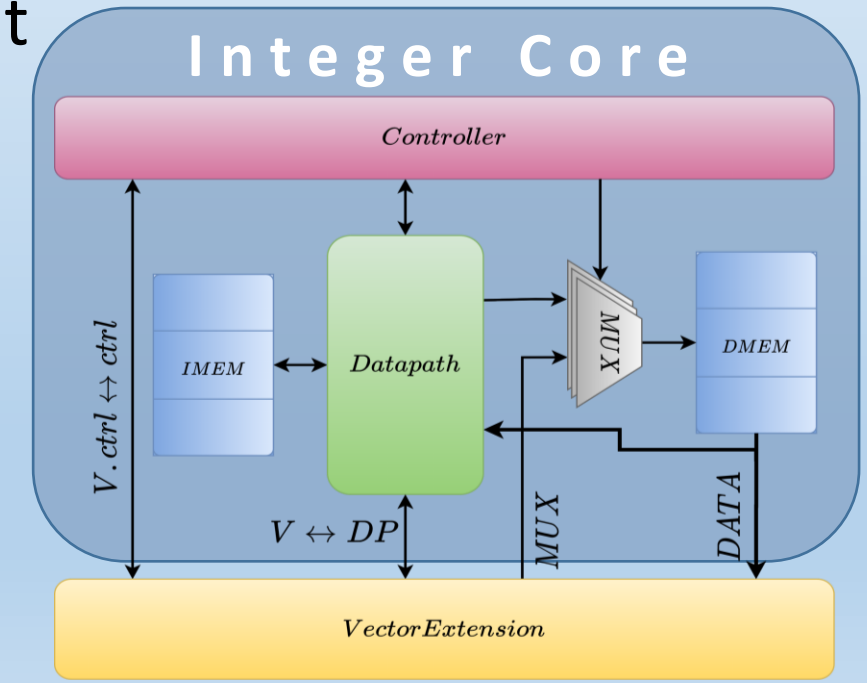
Project Scope

- Explore "*Vector Extension*" in the environment of a RISC-V Multi-Cycle core
- **RISC-V Vector Processor From A to Z:**
  - **Design**
  - **Implement**
  - **Validate**
  - **Evaluate**



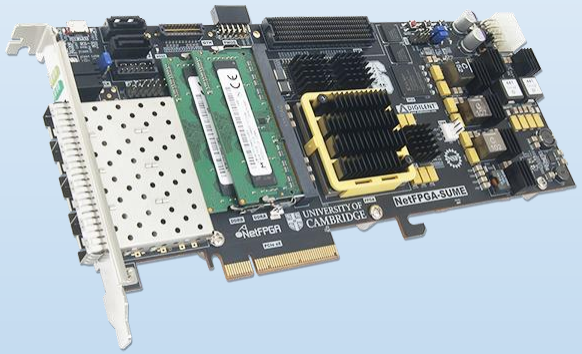
Project Milestones

1) Study and Research
2) Integer Core – Simulative → FPGA
3) Design and Implement a Vector Processing Unit
4) Integration: Vector Unit into the Integer Core
5) Develop a Performance Measurement System
6) Integer Core vs. Vector Processor Comparative Evaluation

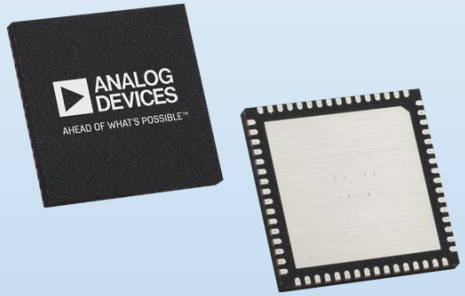


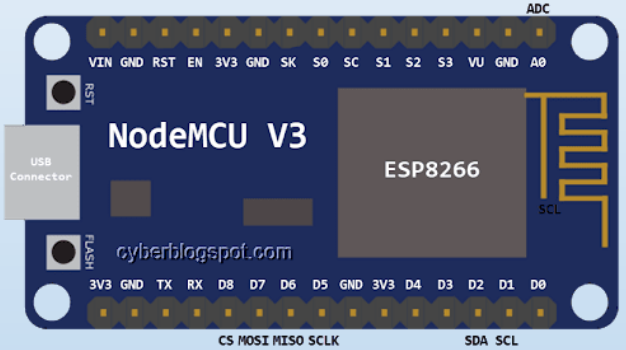
Project Platforms

NetFPGA SUME



Power Meter





VIVADO™

ARDUINO™

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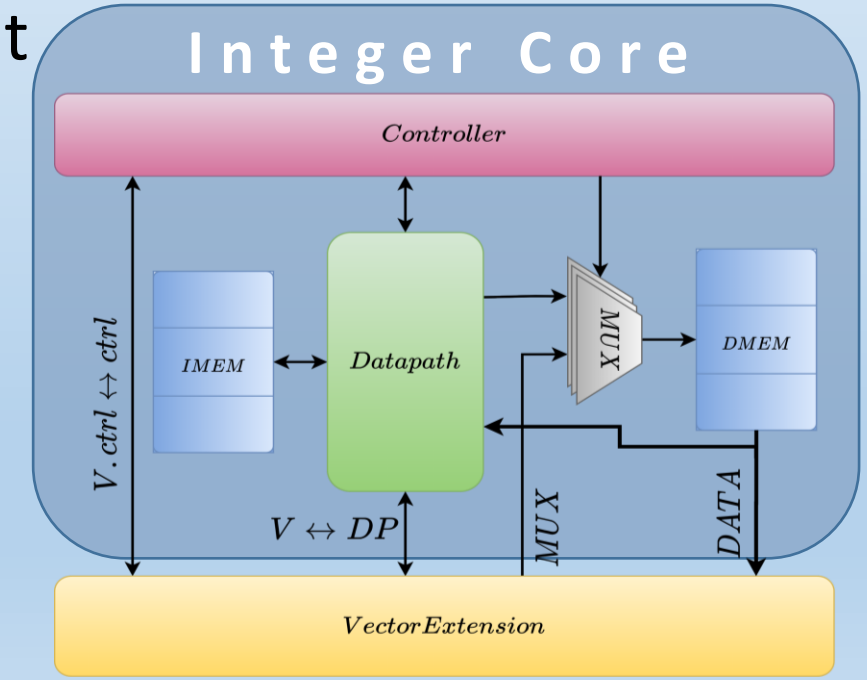

Convert Simulative Core into Synthesizable Core

- Challenges:
  - Memory Block Implementation
  - Syntax Issues
  - Setup and Hold time

Appeared Simple – Reality Proved Us Wrong

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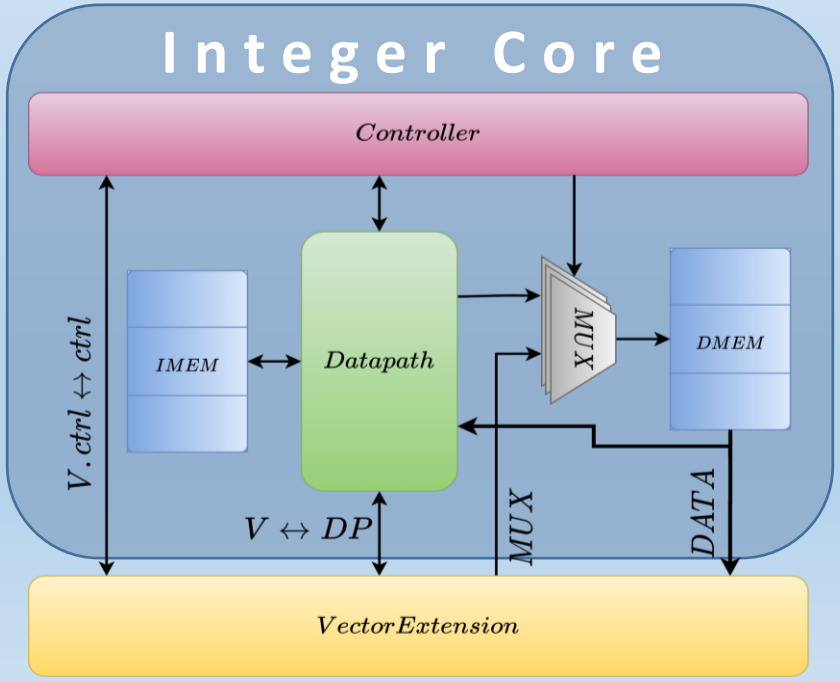

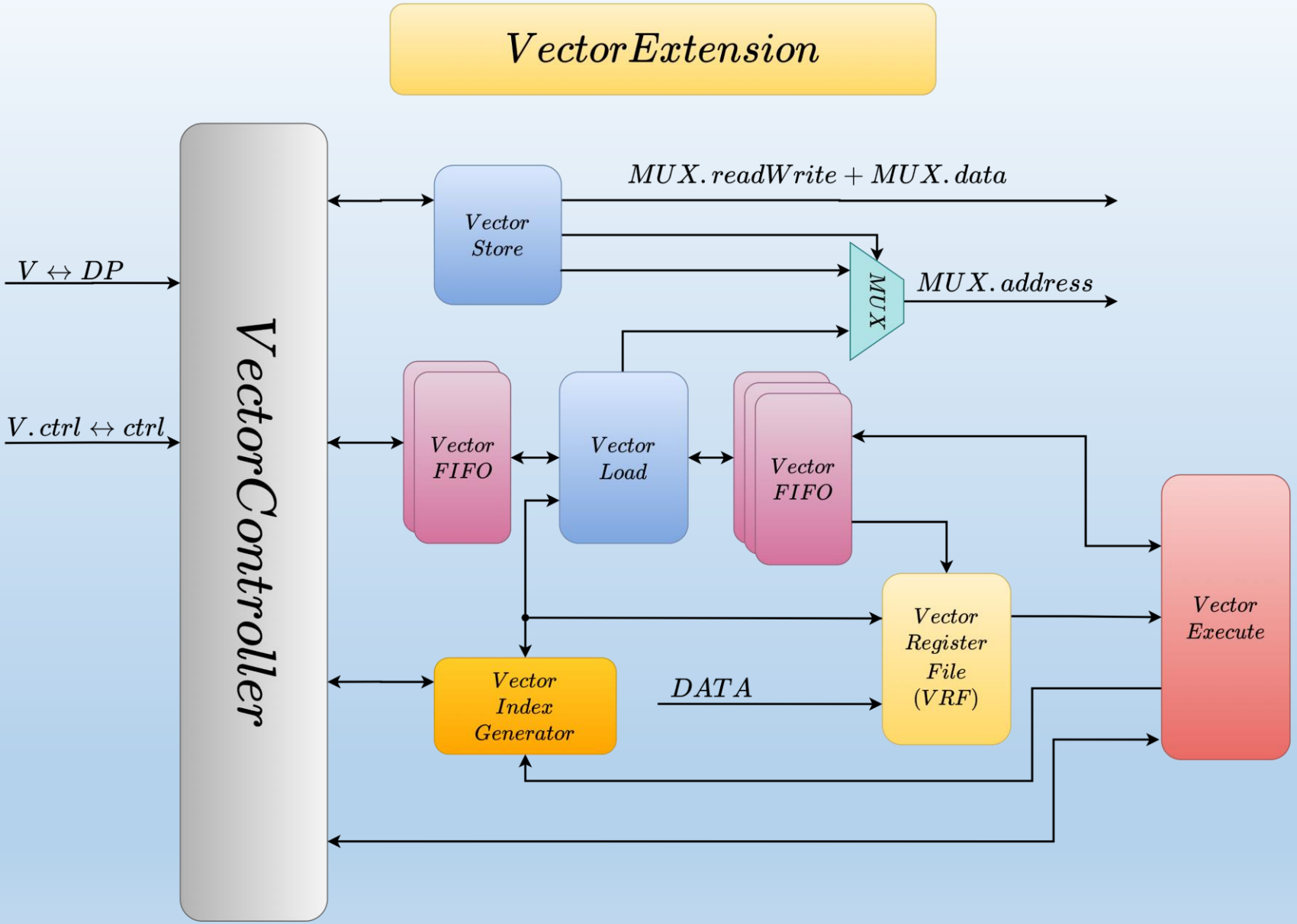
VectorExtension
VectorController
V ↔ DP
V.ctrl ↔ ctrl
Vector Store
MUX.readWrite + MUX.data
MUX
MUX.address
Vector FIFO
Vector Load
Vector FIFO
Vector Register File (VRF)
Vector Execute
Vector Index Generator
DATA

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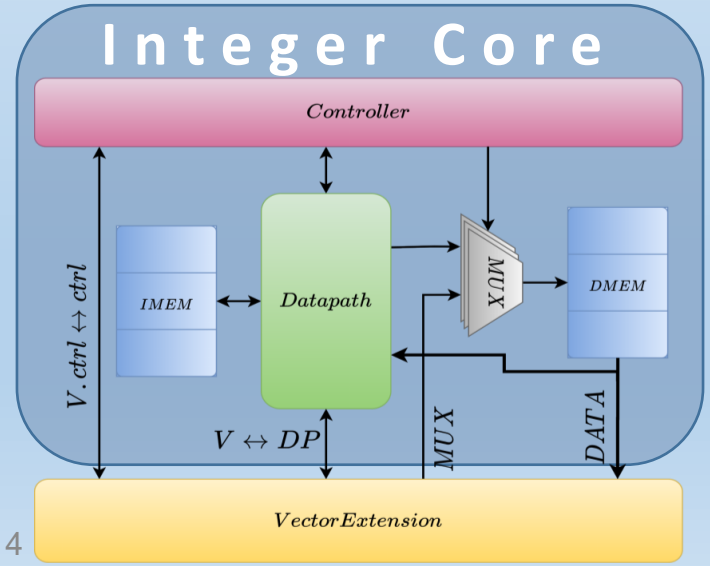
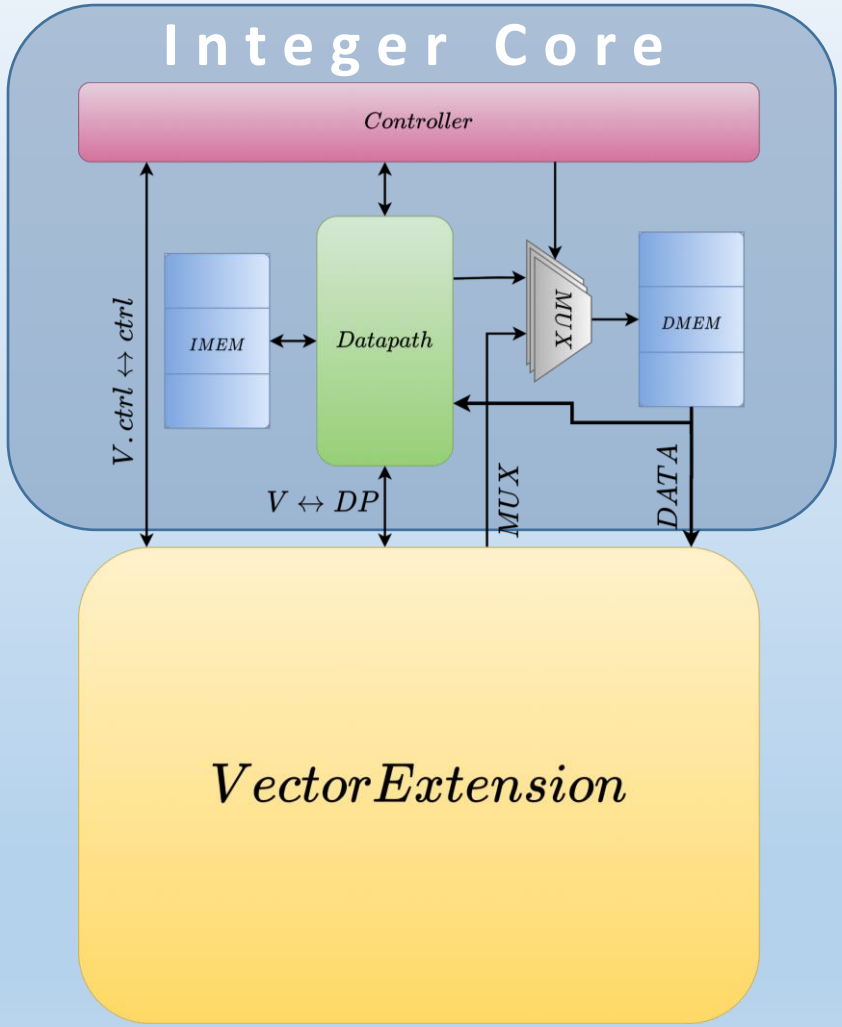
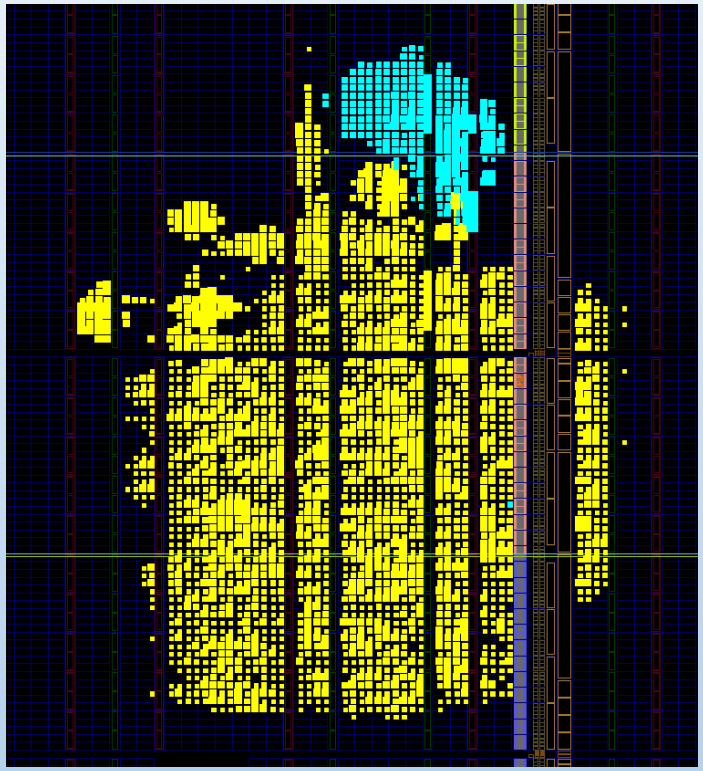


VPU Integration





Large Scale Design + Widespread Integration

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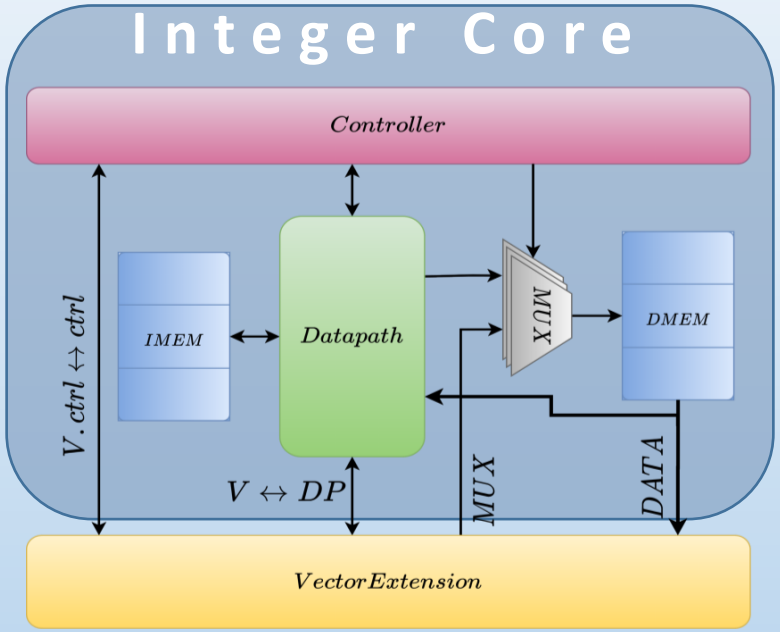


Comparison Parameters

- Hardware Complexity
- Program Execution Time
- Power and Energy

Theoretical Evaluation is Not Enough – True Measurement Required

Performance Measurement System

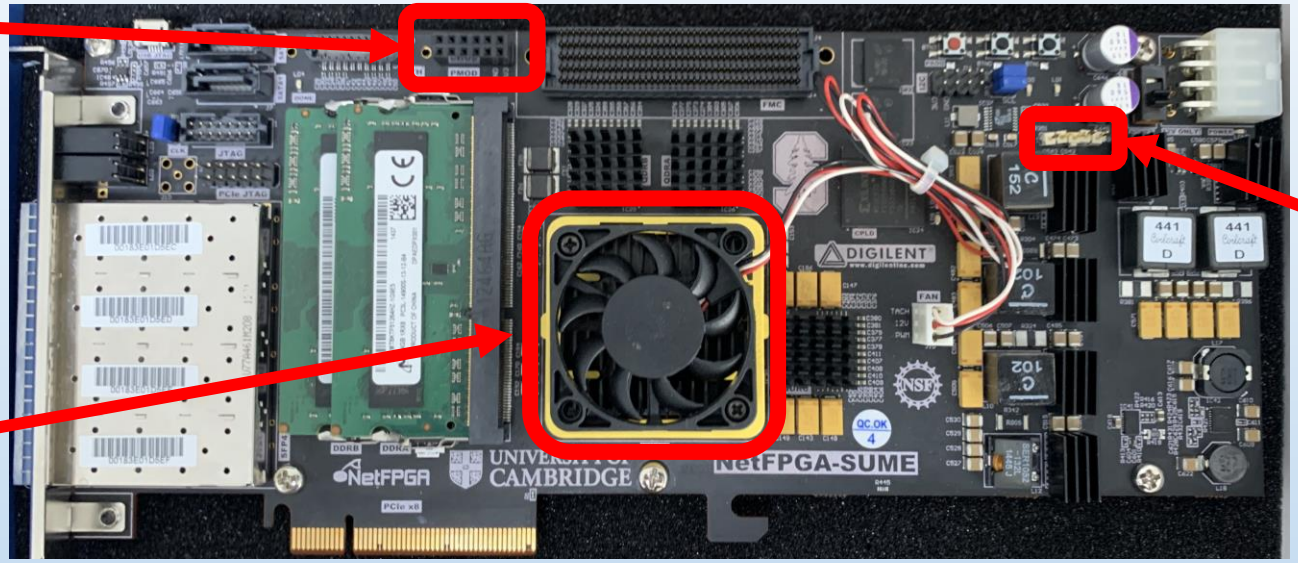
- Actual Power Measurement
- Creating Artificial GPIOs Communication Interfaces
- Study the NetFPGA-SUME Schematics
- Study the Power-Manager datasheet
- Study and implement I^2C Interface

Physical Components

Control Signals

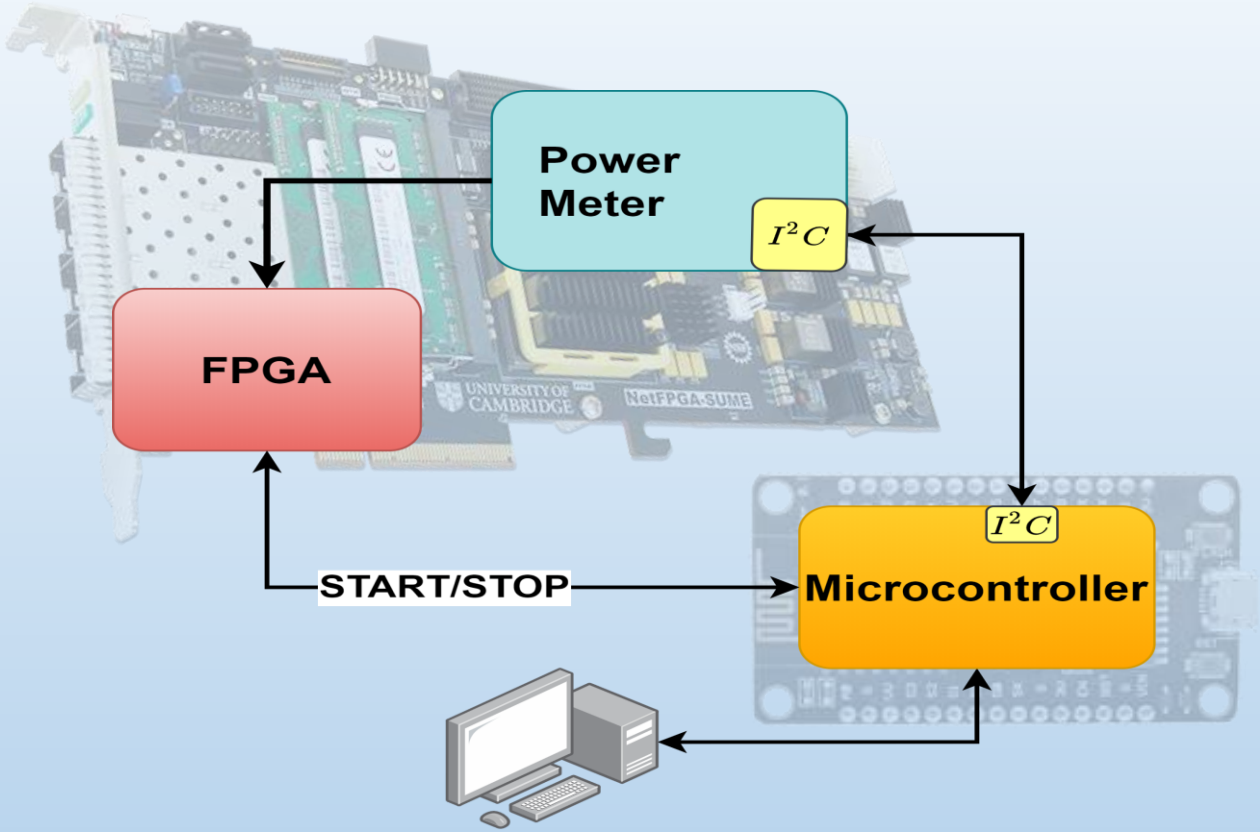
FPGA

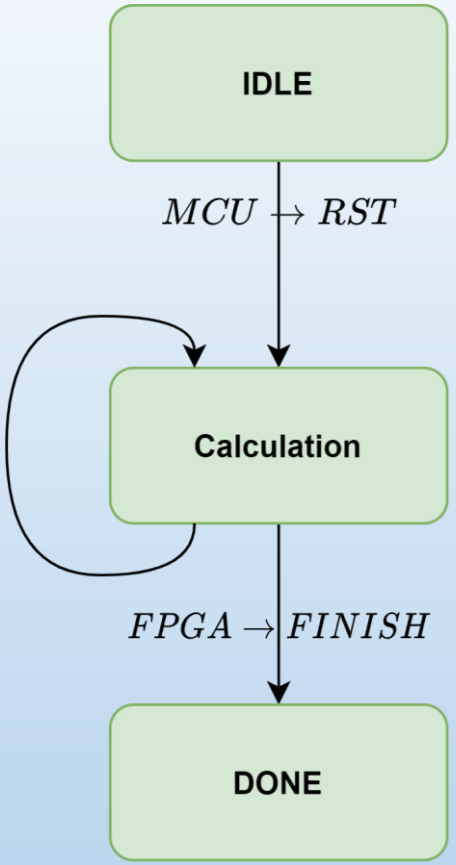
I^2C

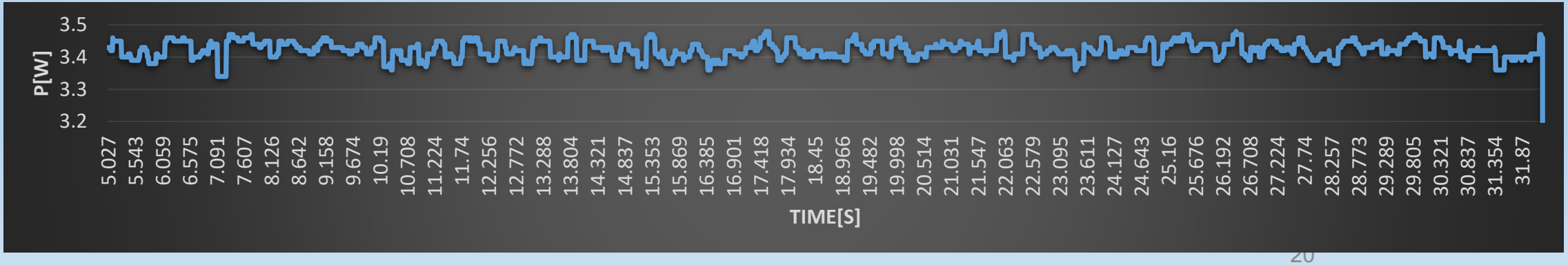


LTC2974 Power Meter

Measurement System







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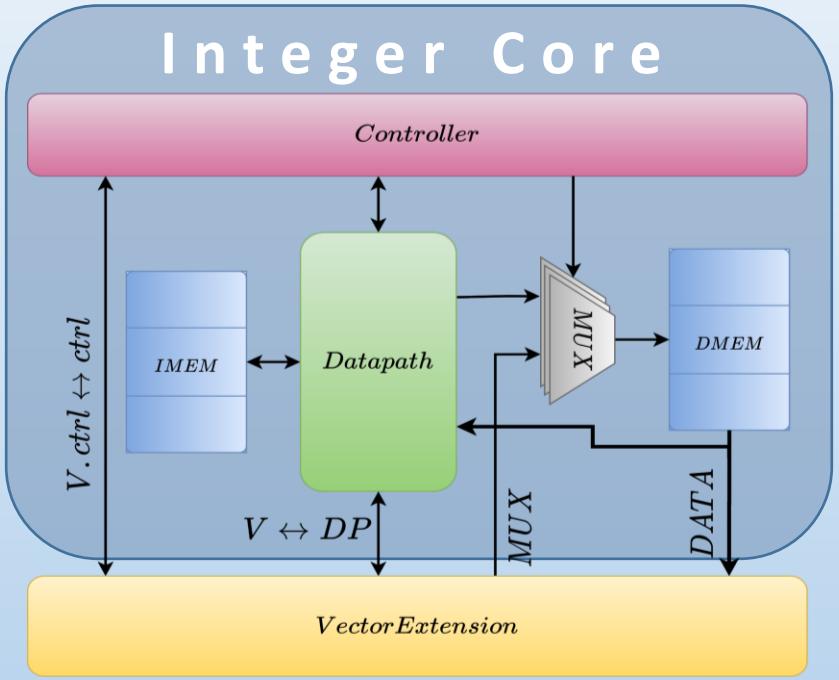


Comparative Evaluation

- Hardware Complexity
- Experimental Results
  - ✓Power
  - ✓Execution Time

Hardware Complexity

Layout – Mapping Onto FPGA Logic

Integer Core

Resource	Utilization
LUT	1350
FF	1295
BRAM	1.50
DSP	3
IO	10
MMCM	1

Vector Processor

Resource	Utilization
LUT	4154
FF	5037
BRAM	1.50
DSP	6
IO	10
MMCM	1
LUTRAM	48

×4 Hardware Complexity

Experimental Results

Benchmark: Inner-Product

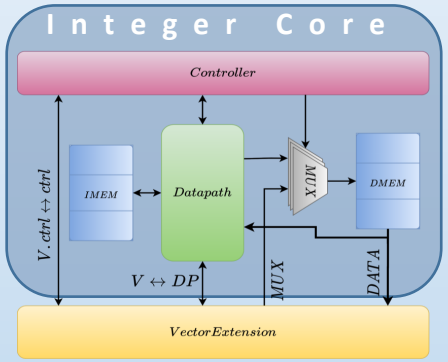
500-element-long-vectors × 1,048,575 times (0xFFFFF)

Experiment No. 1: Single-Core Power Consumption

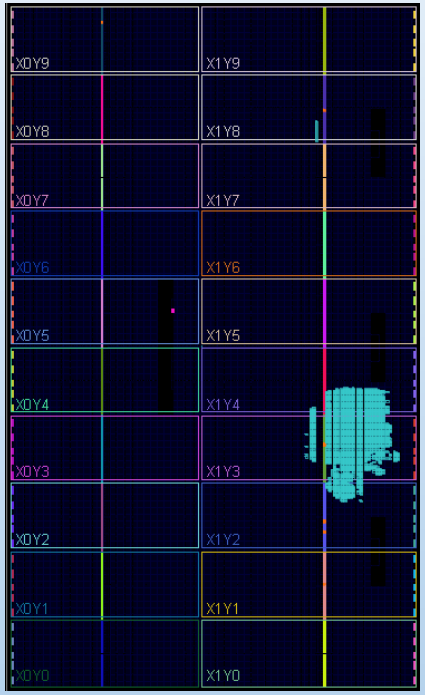
	Integer Processor	Vector Processor
Power	$3.4\ [\mathrm{W}]$	$3.41\ [\mathrm{W}]$
Time Per Program	$325\ [\mu\mathrm{s}]$	$31\ [\mu\mathrm{s}]$

Who are the consumers?

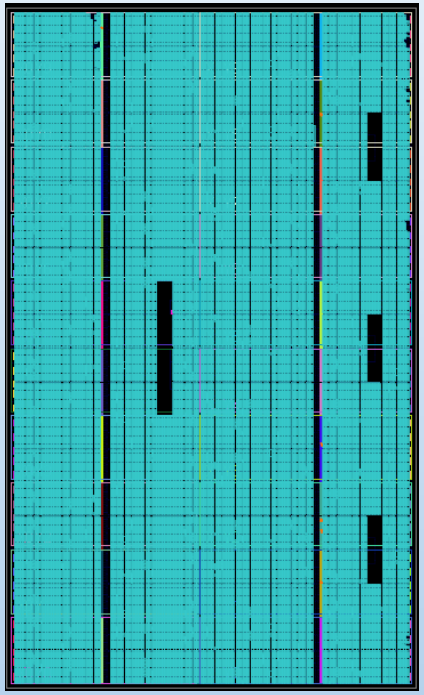
FPGA Resources Utilization

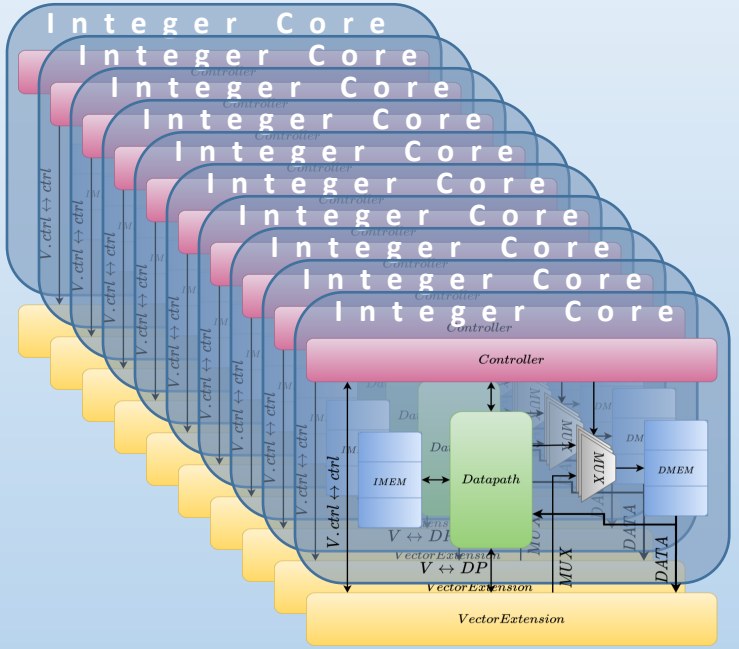


Single-Core



71 Cores





Isolating the Background Consumption

- Hypothesis: Consumption is Linear to Number of Cores
- $Power = P_{background} + \left[P_{single\ core} \times (number\ of\ cores)\right]$

$$(1)\ \underbrace{\boldsymbol{P_{70\ Cores}}}_{\boldsymbol{calculation}} = \underbrace{\boldsymbol{P_{71\ Cores} - P_{1\ Core}}}_{\textbf{measurement}}$$

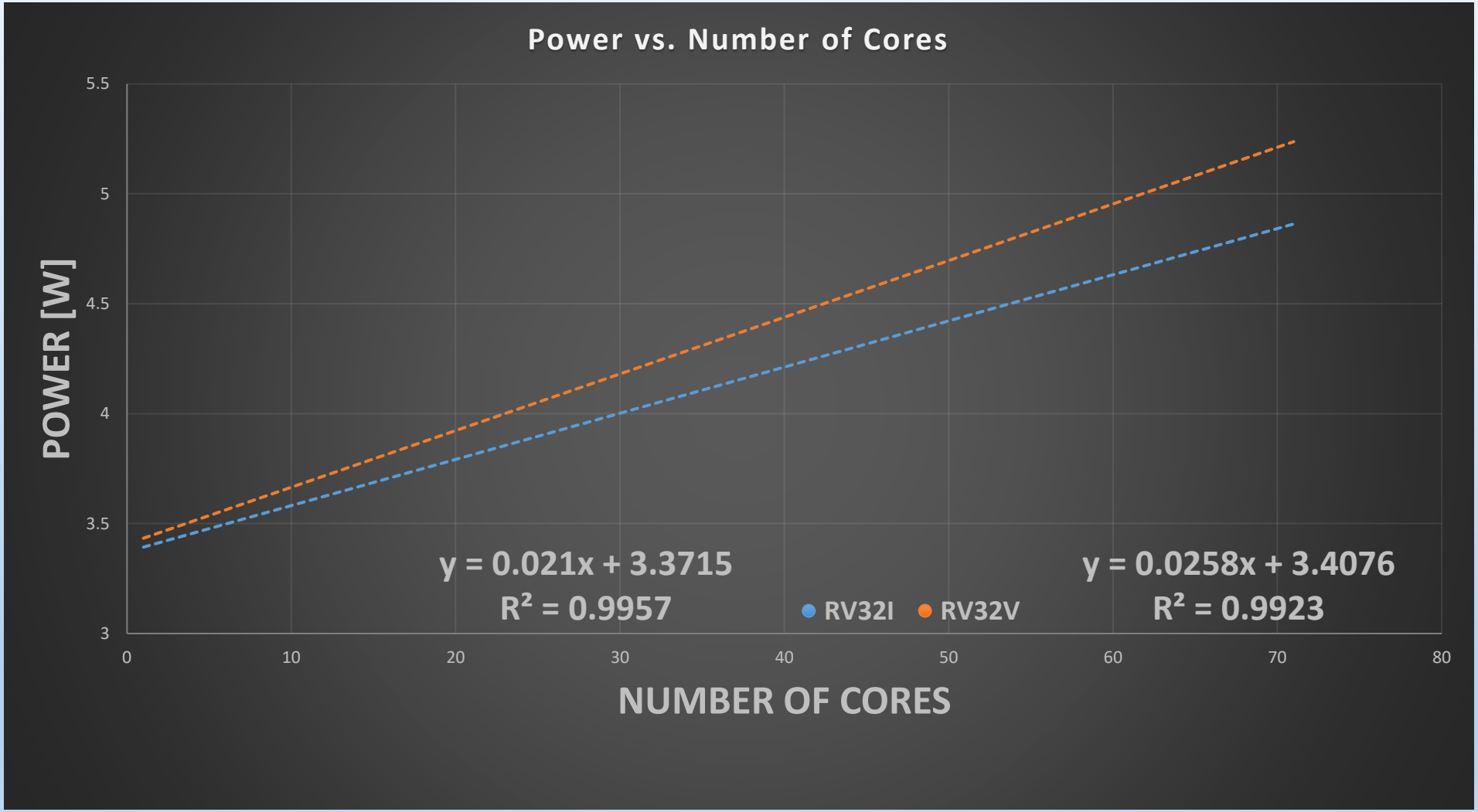
$$(2)\ \boldsymbol{P_{Single\ Core} \approx \frac{P_{70\ Cores}}{70}}$$

Experiment No. 2 – Power Consumption Calculation

	Integer Processor	Vector Processor
Single-Core	3.4 [W]	3.41 [W]
71 Cores	4.9 [W]	5.13 [W]

Power per Core	$21\ [mW]$	$24.6\ [mW]$
Background Power	$3.378\ [W]$	$3.385[W]$

Final Experiment - Hypothesis Confirmation



Indeed Linear Model

Summary of Results

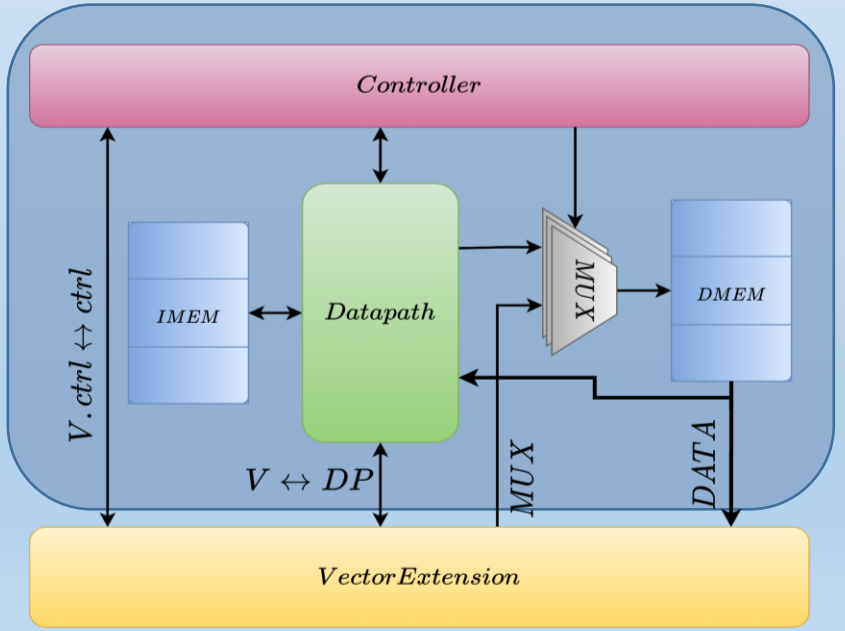
Parameter	Integer Core -RV32I	Vector Processor -RV32V	$\frac{Integer}{Vector}$
Hardware Complexity			0.25
Power	$21\ [mW]$	$26\ [mW]$	0.8
Time Per Program	$325\ [\mu s]$	$31\ [\mu s]$	10.5
Energy Per Program	$6,825\ [nJ]$	$806\ [nJ]$	8.5
Figure of Merit[1]	88.8		

$$Figure\ of\ Merit = \frac{(Time \times Energy)_{RV32I}}{(Time \times Energy)_{RV32V}}$$

[1] - Also known as Energy-Delay Product - $EDP = E \times D = P \times D^2$

Innovation

- We offer a new vector processor structure which has never been explored
- Utilization of a “marginal-advantage” of the non-efficient multi-cycle microarchitecture showed undisputed results



Engineering Difficulties

- Multidisciplinary Project
- Hands-On Experience
- Real Engineering Difficulties Require Real Engineering Solutions

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